Scaling Limits for DRAM

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Abstract:

60-70nm DRAM technologies have been already introduced into mass production. Full process integration results for 50nm DRAM [1], and key technologies for the 40nm DRAM node [2-9] have been presented previously. The data published give confidence that the technical solutions needed for scaling the DRAM technology down to 40nm will be developed in time. For the 30nm node technical concepts are available, however some of the key technologies such as a capacitor dielectric with capacitance equivalent (oxide) thickness (CET) of CET<0.5nm have still to be proven.

In this presentation the key technical challenges for scaling the DRAM one transistor 1 capacitor (1T1C) cell will be discussed, with the focus on the cell structure, the capacitor structure and materials and the cell transistor. The required innovations for the support transistor scaling will be presented. We will also cover new DRAM embedded applications such as SRAM replacement, and new technologies such as floating body (FB) DRAM.