

Scaling Limits for DRAM

Wolfgang Mueller
DRAM Technology
Qimonda Dresden GmbH & Co. OHG, Dresden, Germany

Abstract:

60-70nm DRAM technologies have been already introduced into mass production. Full process integration results for 50nm DRAM [1], and key technologies for the 40nm DRAM node [2-9] have been presented previously. The data published give confidence that the technical solutions needed for scaling the DRAM technology down to 40nm will be developed in time. For the 30nm node technical concepts are available, however some of the key technologies such as a capacitor dielectric with capacitance equivalent (oxide) thickness (CET) of $CET < 0.5\text{nm}$ have still to be proven.

In this presentation the key technical challenges for scaling the DRAM one transistor 1 capacitor (1T1C) cell will be discussed, with the focus on the cell structure, the capacitor structure and materials and the cell transistor. The required innovations for the support transistor scaling will be presented. We will also cover new DRAM embedded applications such as SRAM replacement, and new technologies such as floating body (FB) DRAM.

- [1] T. Tran et al., "A 58nm Trench DRAM Technology", Technical Digest IEDM 2006.
- [2] T. Schloesser et al., "Highly Scalable Sub-50nm Vertical Double Gate Trench DRAM Cell", Technical Digest IEDM 2004.
- [3] W. Mueller et al., "Challenges for the DRAM Scaling to 40nm", Technical Digest IEDM 2005.
- [4] K. Kim, "Technology for sub-50nm DRAM and NAND Flash Manufacturing", Technical Digest IEDM 2005.
- [5] D-G. Park et al., "Stack DRAM Technologies of the Future", Proceedings VLSI TSA 2006.
- [6] W. Mueller et al., "Trench DRAM Technologies for the 50nm Node and Beyond", Proceedings VLSI TSA 2006.
- [7] J.M. Yoon et al., "A Novel Low Leakage Current VPT (Vertical Pillar Transistor) Integration for 4F2 DRAM Cell Array with sub 40nm Technology", Technical Digest 64th Device Research Conference 2006.
- [8] H.P. Moll et al., "Self-Alignment Techniques to Enable 40nm Trench Capacitor DRAM Technologies with 3-D Array Transistor and Single-Sided Strap", Symposium on VLSI Technology 2007, accepted for presentation.
- [9] G. Aichmayr et al., "Carbon/ High-k Trench Capacitor for the 40nm DRAM Generation", Symposium on VLSI Technology 2007, accepted for presentation.
- [10] G. Wang et al., "A 0.127 μm^2 High Performance 65nm SOI Based embedded DRAM for on-Processor Applications", Technical Digest IEDM 2006.
- [11] T. Shino et al., "Floating Body RAM Technology and its Scalability to 32nm Node and Beyond", Technical Digest IEDM 2006.