# Potential and difficulties of GHz processing

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An overview of state of the art Silicon on Insulator CMOS transistors used for 65nm and 45nm volume manufacturing of microprocessors will be given. AMD's unique technology and transistor progression model as well as solutions to lower the power consumption of microprocessor will be described.
For advanced SOI transistors stress engineering has become a standard feature since the 90nm technology node due to gate oxide scaling limitations [1]. Especially techniques which induce local strain such as compressive and tensile stressed over-layer films, embedded-SiGe, and stress memorization, are keys to enhance transistor and product performance. With optimization, the different stressors are highly compatible and additive to each other, improving PMOS and NMOS saturation drive currents by ca. 50% and 30%, respectively [2]. In addition to reducing the lateral and vertical device dimensions advanced (Laser or Flash) annealing has been applied [3]. These anneal processes yield an improved dopant activation for active and gate regions resulting in lower source-drain resistance and gate depletion without any additional diffusion.
To achieve a "high performance per watt", technology and design optimization is required. Technology elements like SOI, stressors, multiple gate oxides needed hand-in-hand development with multiple core designs and power efficient microprocessor architectures. These techniques have been applied and optimized for 65nm and 45nm manufacturing and are scaleable to 45nm design rules. Future technology options, like strained silicon directly bonded on SOI and High K gate oxide will be discussed.

[1] M. Horstmann, et al., IEDM 2005, p. 243
[2] A. Wei et al., VLSI 2007
[3] Th.Feudel et al., RTP Conference, Kyoto, 2006