Channel Engineering on Si-based CMOS Devices

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It has been well recognized that, under sub-100 nm regime, conventional device scaling concept has confronted with several physical and essential limitations. Therefore, any new device engineering to realize advanced CMOS by overcoming these difficulties is strongly needed. A group of theses new device technologies called the technology boosters can be classified mainly into three categories gate stack engineering, source engineering and channel engineering. Particularly, the channel engineering includes carrier-transport-enhanced channels aiming at high current drive and multi-gate channels aiming at high immunity for short channel effects. Among them, the carrier-transport-enhanced channels, typically seen in strained-Si channels, are recently becoming more important.

In this paper, we review our recent results on the development of mobility-enhanced CMOS device structures using strained-Si/SiGe/Ge MOS channels, some of which are combined with multi-gate structures, and the carrier transport properties in those channels. It is shown, particularly, that uniaxial compressive strain and Ge channels are quite effective in pMOS performance enhancement, while uniaxial tensile strain is effective in nMOS performance. Also, the possibility of implementation of III-V materials into channels into n-MOSFETs is briefly addressed. As a result, a device family including strained SOI, SGOI, GOI and III-V-OI structures by global strain or the combination of global and local strain engineering is quite promising for future advanced CMOS.