Thermal crisis of emerging devices/systems and possible solutions

Bruno Michel, IBM Research GmbH, Zurich Research Laboratory, Saeumerstrasse 4,
CH-8803 Rueschlikon, Switzerland, bmi@zurich.ibm.com

Dissipation of kinetic energy from electrons to the structural material is involved in all types of information processing in CMOS and post-CMOS devices, with the power density increasing as function of device density and switching speed. For this reason, heat will be a fundamental problem for nanoelectronics, requiring increased research efforts on heat-flow control in solids, across interfaces, and heat removal by mobile media. The high operation temperatures, which affect device performance and reliability, can only be reduced by drastic reductions of the overall thermal resistance from the point of generation to the heat sink, namely, by a reduction of inherent material resistances, of interface or boundary resistances or phonon reflection, of convective resistances, and of mobile-media heating. Whereas heat generation in current CMOS devices is entirely located in one plane, future devices may even be composed of many 3D stacked layers that multiply the thermal problem and require microscale liquid-cooling devices in between the active layers to prevent a thermal crisis.

The presentation focuses on solutions for better heat transfer through all kinds of interfaces encountered in current and future devices, starting with paste thermal interfaces between chip and cap, which are the current thermal bottleneck in most packages. We have improved these interfaces by controlling the particle stacking by means of nested surface channel designs that create a uniform pressure drop as interface material flows across a rectangular surface. Particles are assembled in a controlled fashion to thermally conducting stacks, which almost eliminate the bulk thermal resistance of this component. As a consequence, the next focus of research efforts is the next limiting factor, namely, the phonon boundary reflectance at solid-solid and solid-fluid interfaces.

The second topic to be discussed is the efficient heat transfer from a solid surface to a moving fluid. Here, we use direct liquid jet impingement coolers with micron-sized jets and drainage channel arrays to improve heat transfer and eliminate thermal interface resistances. With a novel optimized manifold design we keep pressure drop and complexity minimal so that most energy can be focused on reducing the thermal boundary layer in the micron-sized features. With that we maximize heat transfer coefficients to a much higher level than possible before. To further improve the heat transfer capability, we use coolants with added nanoparticles and controlled surface chemistry of the channels and particles.

In our approach, we take a holistic approach, focusing not only on nanoscale transistor devices but also on entire compute systems by defining rules for an electrical thermal co-design. With the improved heat removal capabilities, we enable higher power densities in future compact high-performance systems and also help to improve the energy efficiency owing to shorter electrical interconnects, lower noise levels, and smaller leakage currents.