

Summary Highlights
Session IV

**More of Moore, beyond
down-scaling**

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The University of Tokyo

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Fujitsu Labs



Five speakers

- ❁ Kurt Ronse

- Lithography status for 32nm half pitch node and beyond : immersion, EUVL and alternatives

- ❁ Avik Ghosh

- Devices and Interconnects at the Scaling Limits

- ❁ Manfred Horstmann

- Potential and difficulties of GHz processing

- ❁ Keishi Ohashi

- **Achieving Convergence between Electronics and Photonics**

- ❁ Shinichi Takagi

- Channel Engineering on Si-based CMOS Devices



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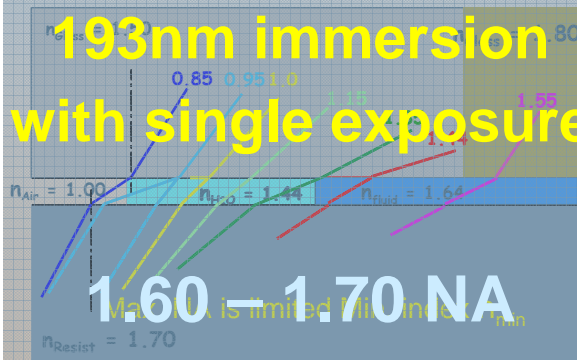
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32nm HP main options

NA-scaling

High index
193nm immersion
with single exposure

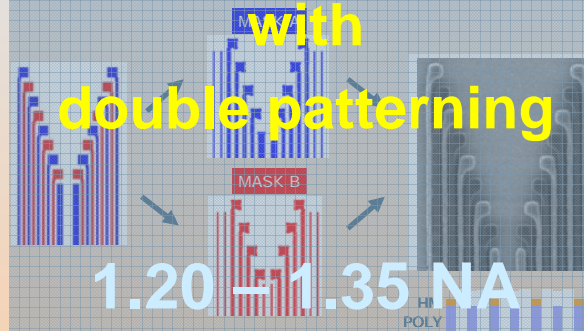


1.60 – 1.70 NA

($k_1 < 0.3$)

k_1 -scaling

ArF Immersion
with
double patterning



1.20 – 1.35 NA

($k_1 = 0.15 - 0.20$)

λ -scaling

Extreme
Ultra-Violet
(EUVL : 13.5 nm)

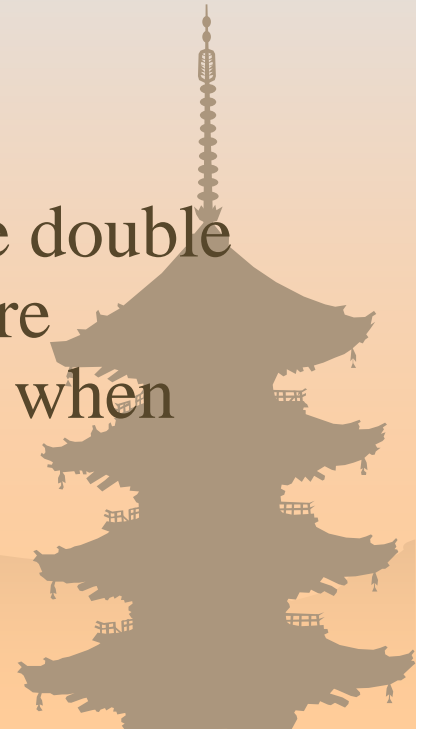


0.25 NA

($k_1 = 0.6$)

Summary (Ronse)

- ❁ Three main patterning routes are still being explored for the 32nm half pitch node
- ❁ Double patterning currently seems to be the most feasible to be ready on time
- ❁ Cost of ownership considerations may cause double patterning to be replaced by a single exposure technique (high index immersion or EUVL) when that is ready



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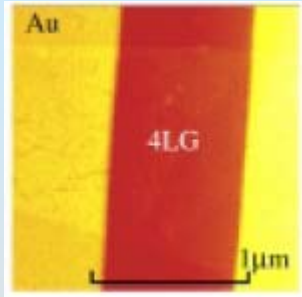


Summary (Ghosh)

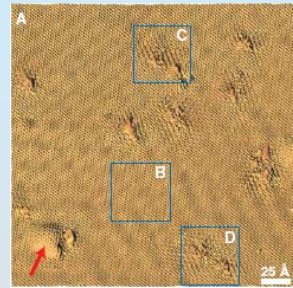
- Theory + Expt suggest that no. of channels \neq no. of valence electrons.
 - Interaction between parallel chains (e.g. bond formation) withdraws some electrons from the conductance process
 - Diff electrons \rightarrow diff. energies/orientations (e.g. s, p_x , p_y , p_z els)
- Fabricating **graphene circuits** out of a common template could circumvent some difficulties of nanotubes (e.g. alignment)
- **Molecular wires** have high resistance (slow), but could offer new features (e.g. conformational gating, trap-assisted tunneling)
- Tunneling ‘Selectivity constraint’ defines lower bound for wire half-pitch ~ 1.5 - 2 nm (for 1 cm wire length and 1 volt operational voltage)
- Tunneling-effected voltage pinning defines another lower bound for the wire half-pitch of about 1.7 nm (for 1 cm wire length and 1 volt operational voltage)



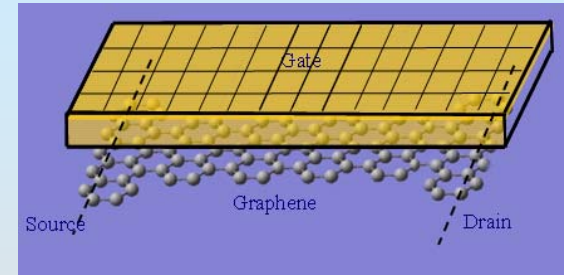
Graphene devices and circuits



Staley et al, preprint
(Litho-free Graphene)

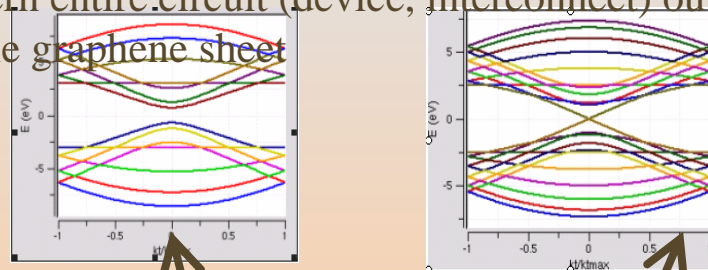


Rutter et al, Science'07
(Epitaxial Graphene on SiC)



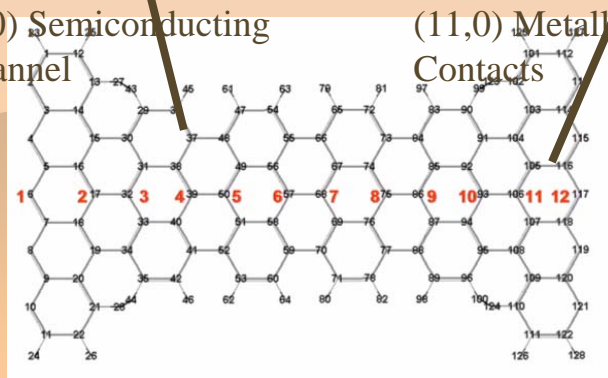
Advantages of CNTs, with perhaps better fabrication, Ohmic contact, superior gate control, alignment

Pattern entire circuit (device, interconnect) out of a single graphene sheet

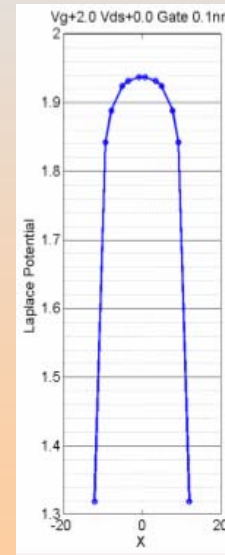


(7,0) Semiconducting Channel

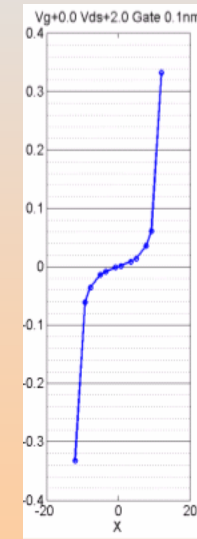
(11,0) Metallic Contacts



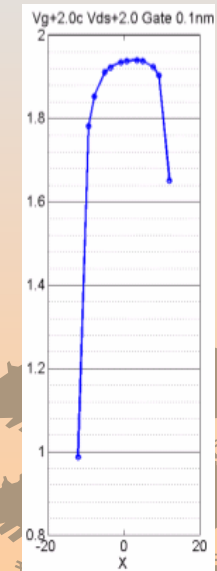
(Unluer, Tsang, Ghosh, Stan, unpublished)



Gate effect



Drain effect
(2D electrostatics)



Gate + Drain

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Summary (Horstmann)

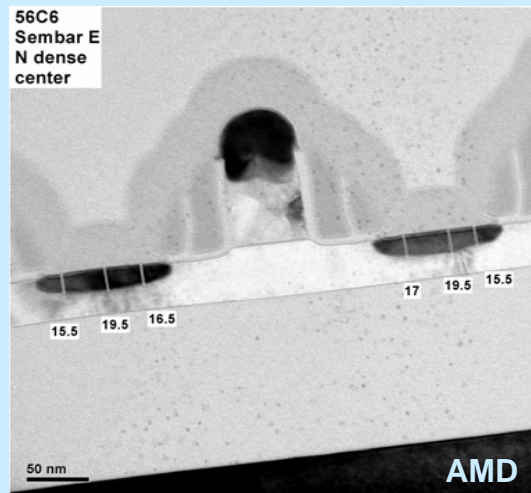
- ❁ For high performance microprocessors **SOI technology** is leading edge
- ❁ **Performance per Watt is key** and power limitations has to be fixed by design and technology – AMD PowerNOW!™, multiple cores, etc.
- ❁ For conventional GOX materials gate and GOX scaling is slowing down and therefore transistor needs other innovations, i.e. **strained Si, more strained Si,.....**
- ❁ Besides stressors, **advanced anneal** is important to reduce diffusion and to minimize parametric variations especially for 45nm/32nm technology nodes
- ❁ On 45nm existing stressors like DSL, SiGe do not fully scale at 45nm pitches.
New stressor materials needed...Si:C, strained SOI
- ❁ High K materials like HfO₂ are the key for the future to keep GOX leakage under control and to allow gate scaling again



Future Transistor Options on SOI...

Optional for 45nm

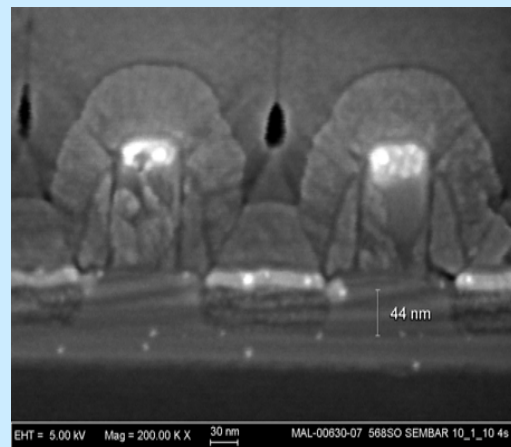
sSOI
(Strained Si directly on SOI)



A.Wei et al., ECS 2006

Optional for 45nm

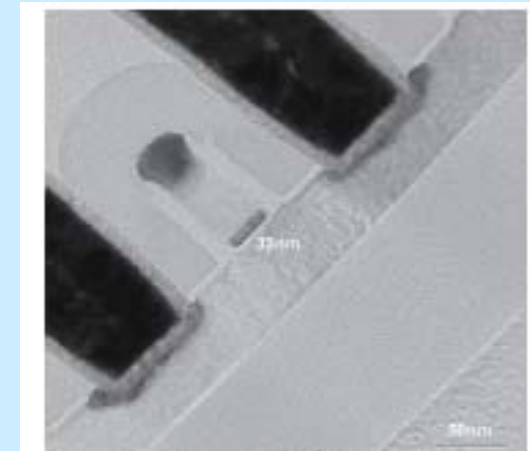
Si:C
(embedded Si:C)



AMD Dresden Q4 2006

Optional for 45nm

High K Gateoxide



M.Chudzik (IBM), M.Hargrove (AMD) et al. VLSI 2007

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Summary (Ohashi)

Si photonics would realize highly integrated optical telecommunication network system.

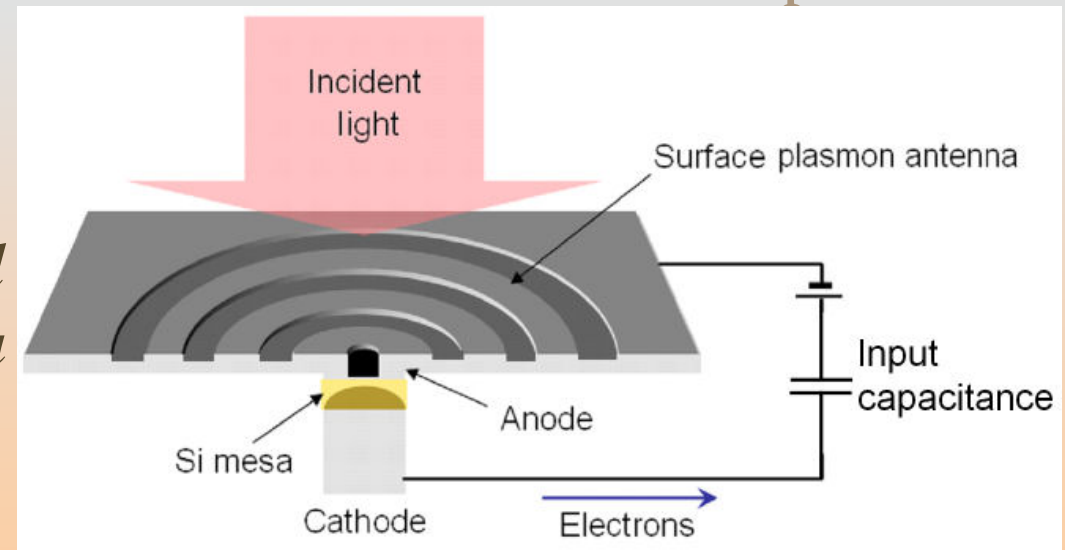
This technology could introduce optical data communication to electronics, if OE/EO elements are fabricated by Si CMOS compatible process.

Nano photonics using the concept of **near-field and surface-plasmons as well as new materials for OE/EO elements will be a key to **achieve convergence between electronics and photonics.****

Si Nanophotodiode

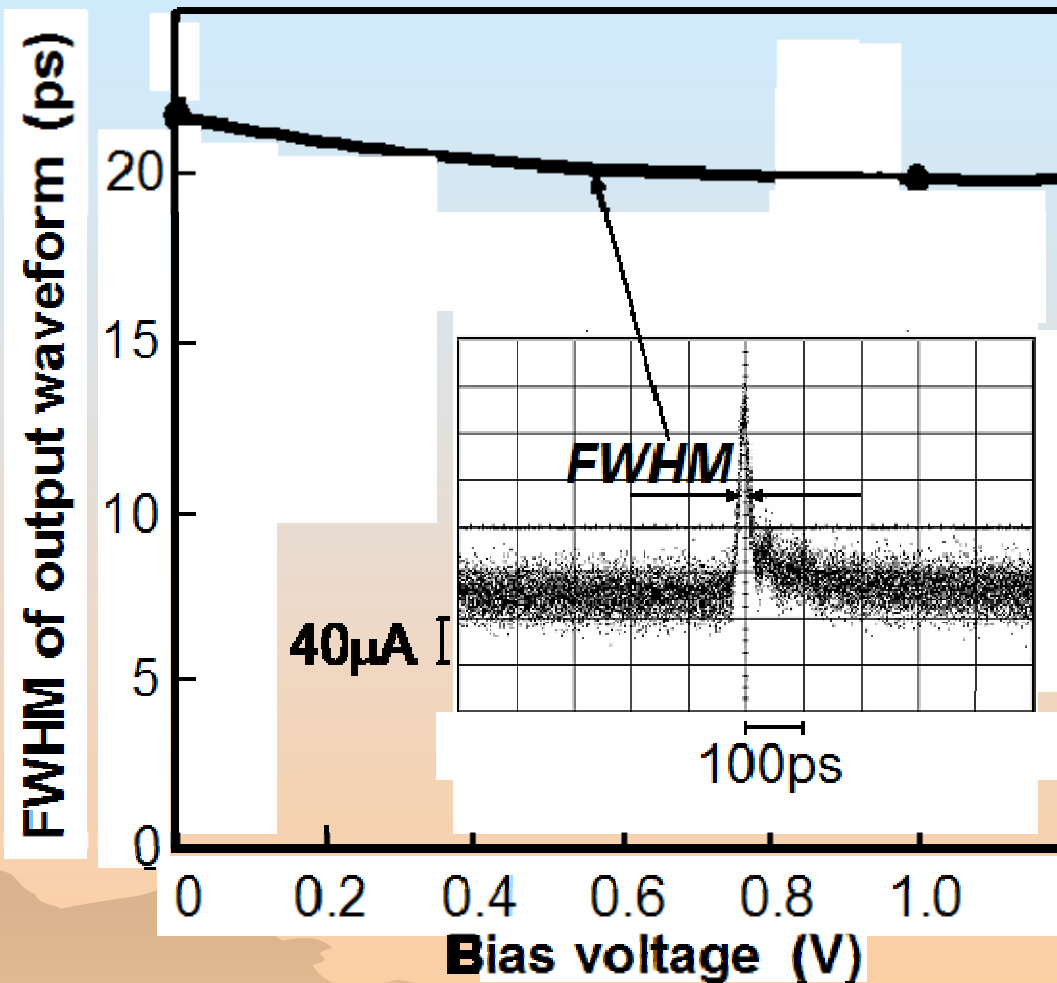
*Application of nano-photonics technology (**surface plasmon antenna**) to electronics*

The light signal is poured from a plasmon antenna to the active region of the Si photodiode.



Size of Si mesa ~ 100 nm

High-Performance Si Nano-Photodiode



- *Fast response*
- *FWHM < 20ps*
- *(>50GHz)*

- *Low bias voltage*
- *0-3 V*

Light Source
Ti-sapphire laser
 $\lambda \sim 800 \text{ nm}$

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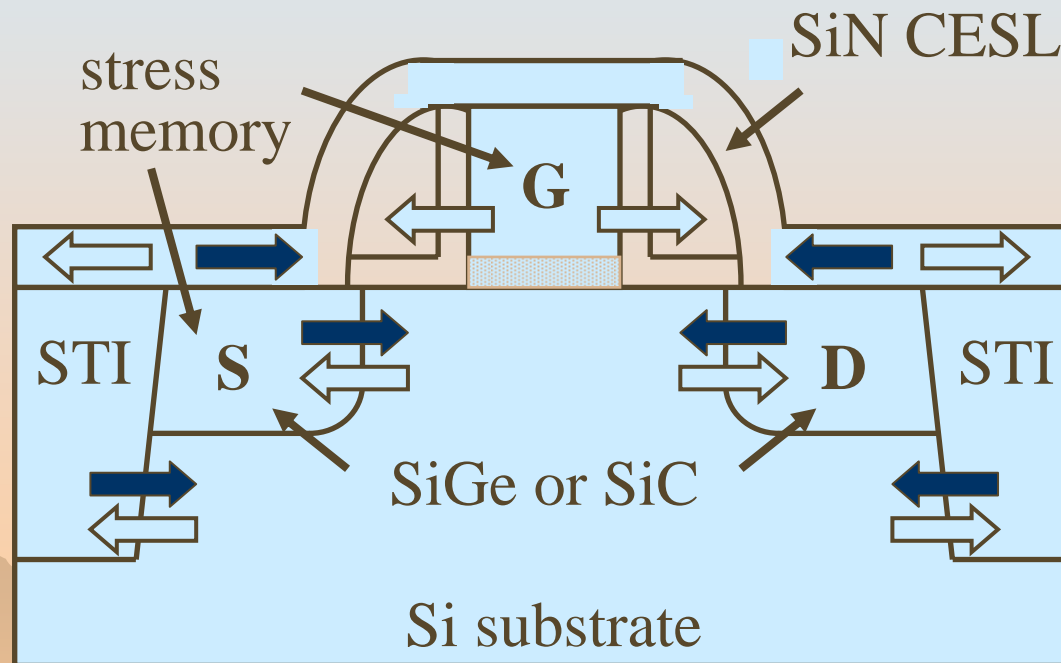
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Si MOSFETs with local strain effects

- SiGe (SiC) Source/Drain → compressive (tensile) strain
- SiN Contact Etch Stop Layers → compressive or tensile strain
- Materials buried into STI → compressive or tensile strain
- Stress memorization of poly Si gate and S/D → tensile strain



➡ Compressive strain
➡ Tensile strain

- Local strain techniques tend to generate strain higher along a specific direction (**uni-axial stress**), because of the geometrical effects

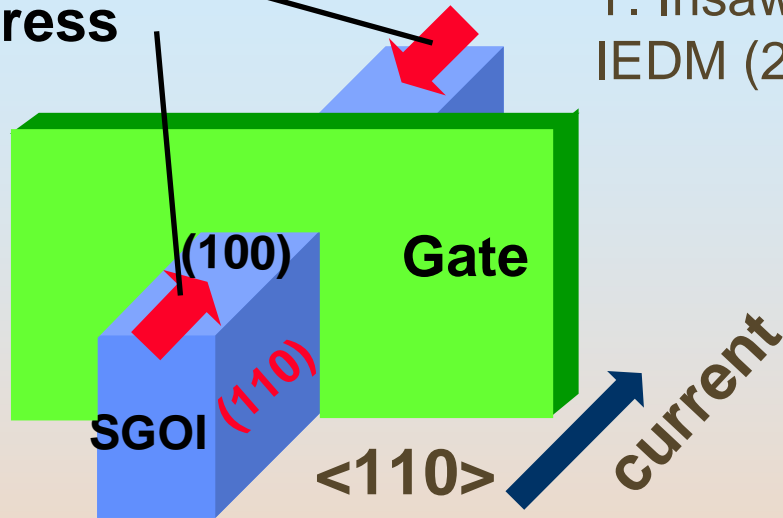
Summary (Takagi)

- ❁ Continuous and successive enhancement of carrier transport properties is needed for boosting the CMOS performance beyond sub 100 nm technology nodes, because of physical limitations on CMOS scaling.
- ❁ For this purpose, **optimization of strain, surface orientation and channel materials** including SiGe, Ge and III-V materials will be pursued through local and global process/device engineering and its combination.
- ❁ **A novel uni-axial compressive strain CMOS** utilizing lateral relaxation and subband engineering for (110) electrons have been proposed and demonstrated.
- ❁ **Compressive strain GOI or Ge wire p-MOSFETs** are expected to provide high current drive and immunity for short channel effects.
- ❁ **III-V MOSFETs** can be employed for low power logic applications by combining with larger bandgap and thicker gate oxides.

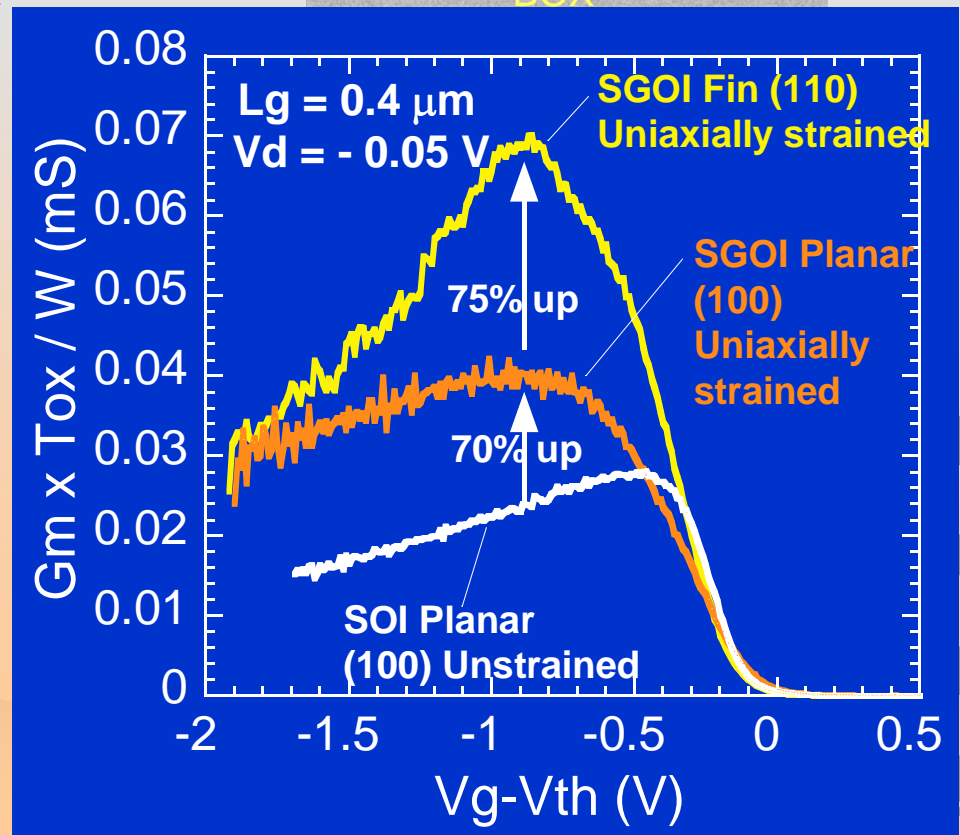
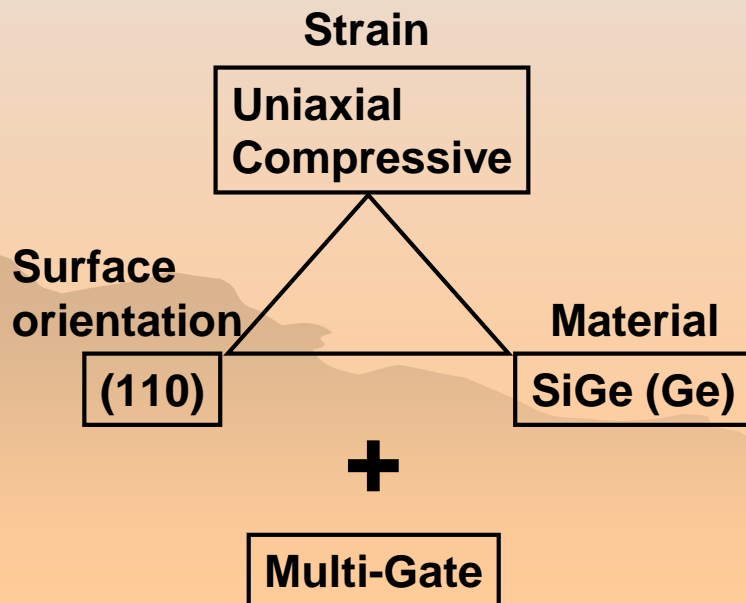
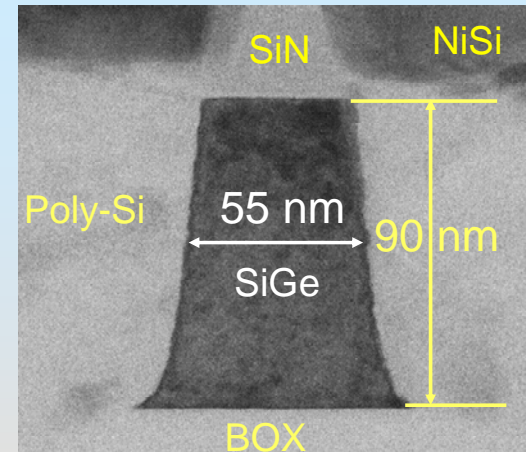


Uniaxially-strained SGOI pMOSFETs

Compressive stress



T. Irisawa et al.,
IEDM (2005) 727



Summary of Session IV

– Technologies Enabling Increased Performance-per-watt

- Lithography
- Strain engineering
- Material engineering including Si/Ge, III-V, Graphene, and molecules
- Integration with photonics using nano-optics such as plasmon and near-field phenomena

– Anything can be on Silicon substrate for the future CMOS technologies

